REMARKS/ARGUMENTS

Claims 1, 4-6, 9, 12-14, and 17-20 are pending in the present application. Claims 1, 6, 9, 14, and 17-20 have been amended; claims 2, 3, 7, 8, 10, 11, 15, and 16 were canceled. Support for the amendments to the claims can be found at least in the previously presented claims 17 and 18. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 101

The Examiner has rejected claims 17-18 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter.

The Examiner has rejected these claims stating:

> The claimed invention is directed to non-statutory subject matter. Claims 17 and 18 are directed to a computer program product in a computer readable medium. This claimed subject matter fails to produce a useful, concrete and tangible result. In view of Applicant's disclosure, specification page 18, lines 13-22, the computer readable medium is not limited to tangible embodiments; the computer readable medium includes transmission-type media , such as communication links, wired or wireless communication links, etc. As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

Final Office Action dated February 06, 2007, p. 3.

Section 101 of Title 35 U.S.C. sets forth the subject matter that can be patented:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

"[N]o patent is available for a discovery, however useful, novel, and nonobvious, unless it falls within one of the express categories of patentable subject matter of 35 U.S.C. § 101." *Kewanee Oil Co.* v. Bicron *Corp.*, 416 U.S. 470, 483, 181 USPQ 673,679 (1974). The statutory categories of § 101 define eligible (patentable or statutory) subject matter, i.e., subject matter that can be patented. The listed statutory categories of invention are "process, machine, manufacture, or composition of matter."

Claim 17 is representative of all claims in this group and recites:

> 17. A computer program product in a computer readable recordable medium for transferring data from a memory to a network adapter, the computer program product comprising:
>
> first instructions for receiving a request to transfer data in the memory to a network adapter;
>
> second instructions for setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line

size, wherein an amount of data is less than or equal to the transfer size, and wherein the amount of data to be transferred is in a frame and has a frame size;

third instructions for setting a valid length indicator, wherein the valid length indicator is set to the amount of data and wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter; and

fourth instructions for, responsive to receiving the request, transferring to the network adapter an amount of data equal to the transfer size.

By making the following amendments and additional reasoning, Applicants supplement the reasoning advanced as to the patentability of claims 17-18 in their previously presented form in the response to the previous non-final office action. Claim 17 has been amended to recite a "recordable medium". Claim 18 has been similarly amended to recite a "recordable medium". Therefore, amended claims 17-18 are directed to statutory subject matter patentable under 35 U.S.C. § 101.

Furthermore, claim 17 has been amended to recite, "a fourth instruction for, responsive to receiving the request, transferring to the network adapter an amount of data equal to the transfer size". This feature of claim 17 transfers data. Transfer of data is a tangible result produced by the invention of claim 17 for the purposes of 35 U.S.C. § 101. Therefore, claim 17 is directed to statutory subject matter patentable under 35 U.S.C. § 101 for this additional reason.

Claim 18 similarly includes a feature, "third instructions for initiating a transfer of data". Initiating a transfer of data invariably transfers data, which is a tangible result. Thus, claim 18 is also similarly directed to statutory subject matter patentable under 35 U.S.C. § 101 for this additional reason. Therefore, the rejection of claims 17-18 under 35 U.S.C. § 101 has been overcome.

II. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1, 4-6, 9, and 12-14 under 35 U.S.C. § 102(b) as being anticipated by *Chen et al*, System for Transferring Length Round Down to Cache Line Multiple Capable to Determine Type of Read Request Which Selects and Reads Portion of Prefetched Data in Memory, United States Patent No. 6,055,580 (issued, April 25, 2000), (hereinafter, "*Chen*"). This rejection is respectfully traversed.

II.A As to claims 1, 4-5, 9, and 12-13

The Examiner has rejected claim 1 stating:

> As for claim 1, Chen et al teach a method in data processing system for transferring [col. 7, lines 62-65] data from a memory [e.g., main memory 104, cache 105] to a network adapter [network interface card 1241, the method comprising:

receiving [col. 7, lines 62-65] a request to transfer data in the memory to a network adapter; and

setting a transfer size to align [col. 3, lines 21-25; col. 3, lines 42-45; col. 9, lines 43-59] the data with a cache line size if the amount of data to be transferred is unequal [col. 3, lines 17-21] to the cache line size, wherein an amount of data is less that or equal to the ,transfer size, and wherein the amount of data to be transferred is in a frame and has a frame size [conformed to PCI system's inherent use of memory line sizes and boundaries, e.g., 32 bytes, during data transfers in col. 9, lines 27-30, col. 11, lines 12-15 or packets in col. 7, lines 2-5 and NDIS packet descriptor (inherently having a packet length) in col. 8, line 65-col. 9, line 6].

Final Office Action dated February 06, 2007, p. 4.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case, each and every feature of the amended claim 1 is not identically shown in the cited reference, arranged as they are in this amended claim.

Amended claim 1 recites:

1. A method in a data processing system for transferring data from a memory to a network adapter, the method comprising:

receiving a request to transfer data in the memory to a network adapter;

setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size, and wherein the amount of data to be transferred is in a frame and has a frame size;

setting a valid length indicator, wherein the valid length indicator is set to the amount of data and wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter; and

responsive to receiving the request, transferring to the network adapter an amount of data equal to the transfer size.

The following reasoning is in addition to the arguments advanced against the anticipation rejection of amended claim 1 over *Chen* in the response to the previous non-final office action. Amended claim 1 has been amended to include a second setting step, namely, "setting a valid length indicator". This step is analogous to the "third instructions for setting a valid length indicator" in the previously

presented claim 17. The Examiner has conceded in the present final office action that *Chen* does not teach the third instructions of claim 17. In rejecting claim 17 in the present final office action, the Examiner states:

> Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. [US 6,055,5801 in view of Webber et al. [US 6,820,186 B2].
>
> As for claim 17, Chen et al teach a computer program product in a computer readable medium for transferring data from a memory [e.g., main memory 104, cache 105] to a network adapter [network interface card 124], the computer program product comprising:
>
> first instructions for receiving [col. 7, lines 62-65] a request to transfer data in the memory to a network adapter; and
>
> second instructions for setting a transfer size to align [col. 3, lines 21-25; col. 3, lines 42-45; col. 9, lines 43-59] the data with a cache line size if the amount of data to be transferred is unequal [col. 3, lines 17-21] to the cache line size, wherein an amount of data is less that or equal to the transfer size, and wherein the amount of data to be transferred is in a frame and has a frame size [conformed to PCI system's inherent use of memory line sizes and boundaries, e.g., 32 bytes, during data transfers in col. 9, lines 27-30, col. 11 ,lines 12-15 or packets in col. 7, lines 2-5 and NDIS packet descriptor (inherently having a packet length) in col. 8, line 65-col, 9, line 6].
>
> However, Chen et at do not explicitly disclose a valid length indicator is set to the amount of data wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter. Webber et al teach transferring data [col. 1, lines 5-19] aligned with a cache line size from a memory to a network adapter in order to build a packet payload to be transmitted on a network and further teach a valid length indicator [col. 2, lines 30-41] is set to the amount of data wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter. At the time the invention was made, one of ordinary skill in the art would have been motivated to combine the cited references in order to increase flexibility by providing a request beginning at arbitrary Webber et al: col. 1, lines 5-19] location of a cache line rather than beginning at a starting address [Chen et al: col. 3, lines 8-11] of a cache line.

Final Office Action dated February 06, 2007, pp. 6-7.

Because the Examiner concedes that *Chen* does not teach the third instructions of claim 17, *Chen* also does not teach the second setting step of the amended claim 1. The Examiner further incorrectly asserts that a secondary reference *Webber et al.*, System and Method for Building Packets, United States Patent No. 6,820,186 (Published, November 16, 2004) (hereinafter, "*Webber*"), teaches or suggests the third instructions of claim 17. As will be shown below with respect to claim 17, *Webber* also fails to teach or suggest the third instructions of claim 17. Consequently, *Chen*, or a combination of *Chen* and *Webber*, fails to teach or suggest all the features of claim 1 arranged as they are in claim 1.

Therefore, the anticipation rejection of claim 1 under 35 U.S.C. § 102(b) has been overcome. Furthermore, claim 17 contains features similar to those in claim 1. Claim 1 is also not obvious over

Chen and *Webber* as will follow from the reasoning as to claim 17 below. Independent claim 9 contains features and amendments similar to those in claim 1, and is also not anticipated or made obvious by *Chen*, or the combination of *Chen* and *Webber* by similar reasoning. Dependent claims 4-5 and 12-13 are also not anticipated or made obvious at least by virtue of their dependence from one of these independent claims.

The Examiner has included the rejection of claim 19 under the obviousness rejection of claims 17 and 18. The Examiner states:

> As for claims 19 and 20, Chen et al teach a method for transferring data from a memory to a network adapter [supra]. Therefore, Chen et al teach the server for performing this method. The present claims are rejected under the same basis.

Final Office Action dated February 06, 2007, p. 9.

From the wording of the Examiner's rejection of claim 19, Applicants surmise that the Examiner meant to reject claim 19 for anticipation by *Chen* and not for obviousness over *Chen* and *Webber*. Therefore, Applicants respond assuming the rejection of claim 19 to be an anticipation rejection under 35 U.S.C. § 102(b) similar to the rejection of claim 1. Independent claim 19 contains features similar to those recited in claim 1. Accordingly, claim 19 is not anticipated by *Chen* by reasoning similar to that advanced as to claim 1 above.

II.B **As to claims 6 and 14**

The Examiner has rejected claim 1 stating:

> As for claim 6, Chen et al teach a method in data processing system for transferring [col. 7, lines 62-65] data from a memory [e.g., main memory 104, cache 105] to a network adapter [network interface card 124], the method comprising:
>
> identifying [col. 8, lines 48-54] a frame size for a transfer of the data from the memory to the network;
>
> setting [col. 9, lines 49-51] a length equal to a cache line size;
>
> if the frame size is divisible by a cache line size without a remainder, setting a valid data length equal to the length field [col. 3, lines 39-45]; and
>
> if the frame size divided by the cache line size results in a remainder, setting a valid data length equal to the length field [col. 3, lines 17-23; col. 3, lines 39-45], wherein the length field is computed as length field = (FLOOR(frame size/CLS)+1)*CLS, wherein CLS is the cache length size [e.g., 32 bytes = (FLOOR((2 bytes in portion 618 of fig. 6)/(32 bytes))+ 1)*(32 bytes).

Final Office Action dated February 06, 2007, p. 5.

Amended claim 6 recites:

> 6. A method in a data processing system for transferring data from a memory to a network adapter, the method comprising:

identifying frame size for a transfer of the data from the memory to the network adapter;

setting a length equal to a cache line size;

if the frame size is divisible by a cache line size without a remainder, setting a valid data length equal to the length field;

if the frame size divided by the cache line size results in a remainder, setting the length field to align the data with the cache line size, wherein the length field is computed as

length field = (FLOOR(frame size/CLS)+1)*CLS,

wherein CLS is the cache length size; and

initiating a transfer of the data from the memory to the network adapter using the valid data length and the length field, wherein the network adapter only outputs data identified by the valid data length.

The following reasoning is in addition to the arguments advanced against the anticipation rejection of claim 6 over *Chen* in the response to the previous non-final office action. Claim 6 has been amended to include initiating a transfer step. This step is similar to the "third instructions for initiating a transfer" in the previously presented claim 18. The Examiner has conceded in the present final office action that *Chen* does not teach the third instructions of claim 18. In rejecting claim 18 in the present final office action, the Examiner states:

> However, Chen et al do not explicitly disclose third instructions for initiating a transfer of the data from the memory to the network adapter using the valid data length and the length field, wherein the network adapter only outputs data identified by the valid data length. a valid length indicator is set to the amount of data wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter. Webber et al teach transferring data [col. 1, lines 5-19] aligned with a cache line size from a memory to a network adapter in order to build a packet payload to be transmitted on a network and further teach third instructions for initiating a transfer of the data from the memory to the network adapter using the valid data length and the length field [col. 2, lines 30-41] wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter.

Final Office Action dated February 06, 2007, p. 8.

Because the Examiner concedes that *Chen* does not teach the third instructions of claim 18, *Chen* also does not teach the initiating a transfer step of the amended claim 6. The Examiner further incorrectly asserts that *Webber* teaches or suggests the third instructions of claim 18. As will be shown below with respect to claim 18, *Webber* also fails to teach or suggest the third instructions of claim 18. Consequently, *Chen*, or a combination of *Chen* and *Webber*, fails to teach or suggest all the features of claim 6 arranged as they are in the amended claim 6.

Therefore, the anticipation rejection of claim 6 under 35 U.S.C. § 102(b) has been overcome. Furthermore, claim 18 contains features similar to those in claim 6. Claim 6 is also not obvious over

Chen and *Webber* as will follow from the reasoning as to claim 18 below. Independent claim 14 contains features and amendments similar to those in claim 6, and is also not anticipated or made obvious by *Chen*, or the combination of *Chen* and *Webber* by similar reasoning.

The Examiner has included the rejection of claim 20 under the obviousness rejection of claims 17 and 18. The Examiner states:

> As for claims 19 and 20, Chen et al teach a method for transferring data from a memory to a network adapter [supra]. Therefore, Chen et al teach the server for performing this method. The present claims are rejected under the same basis.

Final Office Action dated February 06, 2007, p. 9.

From the wording of the Examiner's rejection of claim 20, Applicants surmise that the Examiner meant to reject claim 20 for anticipation by *Chen* and not for obviousness over *Chen* and *Webber*. Therefore, Applicants respond assuming the rejection of claim 20 to be an anticipation rejection under 35 U.S.C. § 102(b) similar to the rejection of claim 6. Independent claim 20 contains features similar to those recited in claim 6. Accordingly, claim 20 is not anticipated by *Chen* by reasoning similar to that advanced as to claim 6 above.

III. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 17-18 under 35 U.S.C. § 103(a) as being unpatentable over *Chen*, in view of *Webber*. The rejection is respectfully traversed.

The Examiner has rejected claims 17 and 18 stating:

> Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. [US 6,055,5801 in view of Webber et al. [US 6,820,186 B2].
>
> As for claim 17, Chen et al teach a computer program product in a computer readable medium for transferring data from a memory [e.g., main memory 104, cache 105] to a network adapter [network interface card 124], the computer program product comprising:
>
> first instructions for receiving [col. 7, lines 62-65] a request to transfer data in the memory to a network adapter; and
>
> second instructions for setting a transfer size to align [col. 3, lines 21-25; col. 3, lines 42-45; col. 9, lines 43-59] the data with a cache line size if the amount of data to be transferred is unequal [col. 3, lines 17-21] to the cache line size, wherein an amount of data is less that or equal to the transfer size, and wherein the amount of data to be transferred is in a frame and has a frame size [conformed to PC1 system's inherent use of memory line sizes and boundaries, e.g., 32 bytes, during data transfers in col. 9, lines 27-30, col. 11 ,lines 12-15 or packets in col. 7, lines 2-5 and NDIS packet descriptor (inherently having a packet length) in col. 8, line 65-col, 9, line 6].
>
> However, Chen et at do not explicitly disclose a valid length indicator is set to the amount of data wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the

network adapter. Webber et al teach transferring data [col. 1, lines 5-19] aligned with a cache line size from a memory to a network adapter in order to build a packet payload to be transmitted on a network and further teach a valid length indicator [col. 2, lines 30-41] is set to the amount of data wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter. At the time the invention was made, one of ordinary skill in the art would have been motivated to combine the cited references in order to increase flexibility by providing a request beginning at arbitrary Webber et al: col. 1, lines 5-19] location of a cache line rather than beginning at a starting address [Chen et al: col. 3, lines 8-11] of a cache line.

Final Office Action dated February 06, 2007, pp. 6-7.

III.A The Cited References Do Not Teach all of the Features of Claims 17 and 18

The Examiner has failed to state a *prima facie* obviousness rejection because the cited references used in proposed combination do not teach all of the features of claims 17 and 18 as believed by the Examiner.

Independent claims 17 and 18 contain different sets of features when each of these claims is considered as a whole. However, these claims contain a common feature, towards which the *Webber* reference is applied. For the purpose of distinguishing this common feature from the teachings and suggestions in *Webber*, claims 17 and 18 are treated together in the reasoning below using claim 17 as an example. Amended claim 17 recites:

> 17. A computer program product in a computer readable recordable medium for transferring data from a memory to a network adapter, the computer program product comprising:
>
> first instructions for receiving a request to transfer data in the memory to a network adapter;
>
> second instructions for setting a transfer size to align the data with a cache line size if the amount of data to be transferred is unequal to the cache line size, wherein an amount of data is less than or equal to the transfer size, and wherein the amount of data to be transferred is in a frame and has a frame size;
>
> third instructions for setting a valid length indicator, wherein the valid length indicator is set to the amount of data and wherein the network adapter outputs only the amount of data set by the valid length indicator after the data has been transferred to the network adapter; and
>
> fourth instructions for, responsive to receiving the request, transferring to the network adapter an amount of data equal to the transfer size.

Contrary to the Examiner's assertion, *Webber* does not teach or suggest the third instructions as recited in claim 17. Particularly, *Webber* fails to teach or suggest that "the valid length indicator is set to the amount of data and wherein the network adapter outputs only the amount of data set by the valid length indicator" as recited in claim 17. The Examiner has asserted a similar rejection towards a similar feature in claim 18.

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). In the case at hand, not all of the features of the claimed invention have been considered and the teachings of the references themselves do not suggest the claimed subject matter to a person of ordinary skill in the art.

The Examiner has cited following sections from *Webber* as teaching this feature of claim 17:

> The memory request logic unit is that portion of a system that sends read requests to the memory **10** for obtaining data to fill a packet payload. When a memory request logic unit **14** receives instructions to build a packet payload, it is given a starting address in memory and a length for the packet payload data. In a system that permits a misalignment between the data for use in the packet payload and the lines of data as stored in memory, the memory request logic unit **14** must determine the shift value. The shift value is the number of bytes from the start of a line in memory to the start of the data for use in the packet payload.

Webber, col. 2, ll. 30-41.

In this section, *Webber* teaches that data is organized in the memory according to memory lines. Lines of memory may be envisioned as blocks of memory. *Webber* teaches that the data needed to build a packet may not begin where a memory line begins. To wit, data for a packet may begin somewhere after the beginning of a memory line. Here, *Webber* teaches that the memory request logic unit, which receives the instructions to build the data packet, must determine where in the memory line the data for the packet begins. Towards this end, the memory request logic unit must set a shift value to indicate how much to shift the reading of the delivered memory line from the beginning of the memory line. For example, if a memory line begins at address 00000000 and the data for the packet begins at 00000005, assuming each increment in the address represents one byte of data, the shift value will be 5. Thus, knowing the shift value, the memory request logic unit will start reading the data for the packet from the sixth byte into the memory line. This teaching, however, fails to teach or suggest "the valid length indicator is set to the amount of data and wherein the network adapter outputs only the amount of data set by the valid length indicator" as recited in claim 17.

Notice that the claim recites a "valid length indicator" indicating a valid length, not an offset or shift as taught by *Webber*. In the above example used for explaining *Webber's* teaching, if the request was for a data packet of 7 bytes, the valid length indicator according to the claim would reflect a value of 7, whereas *Webber* would set the shift value to 5. *Webber* teaches where to start reading in a given memory line. The claim recites "the valid length indicator is set to the amount of data and wherein the

network adapter outputs only the amount of data set by the valid length indicator". Knowing the starting point does not teach or suggest how much to read. Therefore, contrary to the Examiner's belief, *Webber* fails to teach or suggest the third instructions as recited in claim 17.

The Examiner has conceded that *Chen* does not teach this feature. Claim 18 contains a feature that is analogous to this third instruction feature of claim 17. Consequently *Chen* in view of *Webber* fails to make claims 17 and 18 obvious under 35 U.S.C. § 103(a).

III.A.i The Examiner Has Not Stated a Proper Teaching, Suggestion or Motivation to Combine the References, and None Exists

In addition, a *prima facie* obviousness rejection against claim 17 has not been made because no proper teaching or suggestion to combine the references has been stated. A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the combination. *In re Napier*, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed. Cir. 1995); *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990). No such teaching or suggestion is present in the cited references and the Examiner has not pointed out any teaching or suggestion that is based on the prior art.

Instead, the Examiner has only stated a proposed advantage to combining the references. However, an advantage is not necessarily a teaching, suggestion, or motivation. To constitute a proper teaching, suggestion, or motivation, the Examiner must establish that one of ordinary skill would both recognize the advantage and have a reason to implement the advantage.

In the case at hand, the Examiner has not provided a sufficient reason why one of ordinary skill would recognize the proposed advantage or have a reason to implement it. The Examiner first states that a combination of *Chen* and *Webber* would have been obvious "to increase flexibility by providing a request beginning at arbitrary location of a cache line rather than beginning at a starting address of a cache line". Towards this alleged motivation, the Examiner cites a part of the "Background of the Invention" section of *Webber's* disclosure and a part of the "Background of the Invention" section of *Chen's* disclosure. *Webber's* background section provides:

> Many system busses are cache line-oriented and do not support memory requests beginning at arbitrary byte locations. Each memory request fetches an entire cache line by addressing the first byte of the line. Packets transmitted on a network, however, include a payload of data which can begin at any arbitrary byte address. Thus, if the packet payload is to begin with a byte of data in the middle of a cache line, extra complexity is involved in building a packet. When data is returned from memory as a line, the network adapter needs to be instructed to copy only the desired data into a temporary buffer which we call

> herein a packet buffer. A packet buffer is organized with lines of data beginning at the first byte of the packet payload which is not necessarily the first byte of a cache line.

Webber, col. 1, ll. 6-19.

This section identifies the problem that the data for a packet may not begin at a cache line. Recall that *Webber* provides a complete solution to this identified problem by using a shift value as described above.

Chen's background section provides:

> In most PCI-based systems, CPU controlled prefetching operations are based on memory line boundaries, such as, cache line boundaries. That is, in conventional operations such as memory read (MR), memory read line (MRL), and memory read multiple (MRM) operations, data is prefetched from a starting address up to a cache line.

Chen, col. 3, ll. 6-11.

In this section, *Chen* informs that memory read and write is performed along cache lines, starting at a starting address up to a cache line. *Chen* then provides a method for reading data from a memory such that the read operations read until the end of the cache line.

It is evident from the two citations that the two references recognize that the data is arranged in the memory along cache lines. *Webber* reads a full cache line for its application. *Chen* also reads a full cache line for its application. *Webber* provides a method for using the data from a different starting position within the read cache line than the starting address of the cache line. *Chen* provides reading the entire cache line.

From these express teachings, the Examiner extrapolates that the two references combined together provide a motivation "to increase flexibility by providing a request beginning at arbitrary location of a cache line rather than beginning at a starting address of a cache line". Note that the alleged objective driving the motivation identified by the Examiner, is an objective already achieved by *Webber*. In essence, the Examiner suggests that one of ordinary skill in the art would read *Webber's* disclosure, understand what *Webber's* invention does and accomplishes, and then combine Webber with *Chen* to realize and accomplish exactly that function, which *Webber* already accomplishes. This assertion of motivation to combine is absurd and not a motivation at all. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claims 17 and 18.

IV. Conclusion

Applicants respectfully urge that the subject application is patentable over *Chen* and *Webber*, and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: May 7, 2007

Respectfully submitted,

/Rakesh Garg/

Rakesh Garg
Reg. No. 57,434
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Agent for Applicants